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(71)Applicant : HITACHI LTD

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ISHIBASHI KOICHIRO

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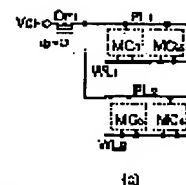
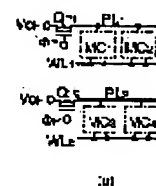
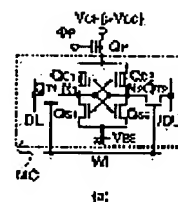
Priority number : 07136349 Priority date : 02.06.1995 Priority country : JP

(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To suppress the increase in sub-threshold current and drop of voltage margin by making a voltage difference between two memory nodes in a memory cell in a non-selection state to be larger than that at the time when the memory cell is selected and a voltage corresponding to writing information is applied.

SOLUTION: A p channel MOSQP, which functions as a switch between a common source for P channel MOSs QC1 and QC2, high potential power supply node for a memory cell MC, and a power supply VCH, is inserted in the memory cell. A common source for N channel MOSs QS1 and QS2, power supply node for on the low-potential side for the memory cell MC, are connected with a reference potential VSS (ground potential is OV normally). When a data is written from a data symmetry to the memory cell, a potential VCC is normally applied to one of the symmetry and a potential 0 to the other thereof respectively in a state where QP is switched off.



LEGAL STATUS

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